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DATE: Sunday, December 12, 2004

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		DB=USPT; PLUR=YES; OP=ADJ	
☐	L20	L19 and (uv or ultraviolet)	39
☐	L19	photoresist with remov$ and (low k) and (inert or nitrogen) with (purg$ or atmosphere)	92
☐	L18	L17 and (low k)	1
☐	L17	l16 and (uv or ultraviolet)	3
☐	L16	(4331485| 4356384| 4680451| 5238878| 5358740| 5705232| 5965047| 5972803| 6033728| 6051512| 6066574| 6107357| 6133550| 6214748| 6225238)![pn]	15
☐	L15	L14 and (uv or ultraviolet)	4
☐	L14	5705232	6
☐	L13	L12 and uv	1
☐	L12	L11 and (low k)	1
☐	L11	6015759.pn. or 5705232.pn.or 5970384.pn.	3
☐	L10	L9 with (UV or ultraviolet)	1
☐	L9	L1 with (dry$ or remov$)	262
☐	L8	L1 same ((drying or remov$) same (uv or ultraviolet))	9
☐	L7	L4 and (134/$.ccls. or 34/$.ccls.)	5
☐	L6	L1 and ((drying or remov$) same (uv or ultraviolet) same temperature same pressure)	3
☐	L5	L1 and ((drying or remov$) same (uv or ultraviolet) same temperature same vacuum)	0
☐	L4	L3 and temperature and vacuum	65
☐	L3	L1 and ((drying or remov$) same (uv or ultraviolet))	117
☐	L2	L1 and drying	156
☐	L1	low k dielectric	1685

END OF SEARCH HISTORY

L20: Entry 19 of 39 File: USPT Jun 24, 2003

DOCUMENT-IDENTIFIER: US 6583497 B2
TITLE: Surface treatment of c-doped SiO2 film to enhance film stability during O2 ashing

Abstract Text (1):
A method for forming an insulation layer over a substrate. The method forms a carbon-doped silicon oxide layer by thermal chemical vapor deposition using an organosilane. The carbon-doped silicon oxide layer is subsequently cured and densified. In one embodiment, the cured film is densified in a nitrogen-containing plasma. The method is particularly suitable for deposition of low dielectric constant films, i.e., where k is less than or equal to 3.0. Low-k, carbon-doped silicon oxide methylsilane or di-, tri-, tetra-, or phenylmethylsilane. and ozone. The above method can be carried out in a substrate processing system having a process chamber; a substrate holder, a heater, a gas delivery system, and a power supply, all of which are coupled to a controller. The controller contains a memory having a computer-readable medium with a program embodied for directing operation of the system in accordance with above method.

Parent Case Text (2):
The instant application claims priority as a divisional application from U.S. patent application Ser. No. 09/633,495, filed Aug. 7, 2000. This application is related to concurrently filed U.S. application Ser. No. 09/625,911, entitled "THERMAL CVD PROCESS FOR DEPOSITING A LOW DIELECTRIC CONSTANT CARBON-DOPED SILICON OXIDE FILM," having Li-Qun Xia, Fabrice Geiger, Frederic Gaillard, Ellie Yieh and Tian Lim as coinventors; and to concurrently filed U.S. application Ser. No. 09/633,196, entitled "METHOD AND APPARATUS TO ENHANCE PROPERTIES OF Si--O--C LOW K FILMS," having Li-Qun Xia, Frederic Gaillard, Ellie Yieh and Tian H. Lim as coinventors; and to concurrently filed U.S. application Ser. No. 09/632,669, entitled "POST-DEPOSITION TREATMENT TO ENHANCE PROPERTIES OF Si--O--C LOW K FILMS," having Li-Qun Xia, Frederic Gaillard, Ellie Yieh and Tian H. Lim as coinventors; and to concurrently filed U.S. application Ser. No. 09/633,798, entitled "LID COOLING MECHANISM FOR OPTIMIZED DEPOSITION OF LOW-K DIELECTRIC USING TRI METHYLSILANE-OZONE BASED PROCESSES," having Himansu Pokharna, Li-Qun Xia and Tian-Hoe Lim as coinventors. Each of the Ser. Nos. 09/625,911, 09/633,196, 09/632,669, and 09/633,798 applications listed above are assigned to Applied Materials, Inc., the assignee of the present invention and each of the above-referenced applications are hereby incorporated by reference.

Brief Summary Text (4):
Semiconductor device geometries have dramatically decreased in size since such devices were first introduced several decades ago. Today's

fabrication plants are routinely producing devices having 0.25 .mu.m and even 0.18 .mu.m feature sizes, and tomorrow's plants soon will be producing devices having even smaller geometries. In order to further reduce the size of devices on integrated circuits, it has become necessary to use conductive materials having low resistivity and insulators having a low dielectric constant. Low dielectric constant films are particularly desirable for premetal dielectric (PMD) layers and intermetal dielectric (IMD) layers to reduce the RC time delay of the interconnect metalization, to prevent cross-talk between the different levels of metalization, and to reduce device power consumption. Undoped silicon oxide films deposited using conventional CVD techniques may have a dielectric constant (k) as low as about 4.0 or 4.2. One approach to obtaining a lower dielectric constant is to incorporate fluorine in the silicon oxide film. Fluorine-doped silicon oxide films (also referred to as fluorine silicate glass or--"FSG" films) may have a dielectric constant as low as about 3.4 or 3.6. Despite this improvement, films having even lower dielectric constants are highly desirable for the manufacture of integrated circuits using geometries of 0.18 .mu.m and smaller. Numerous films have been developed in attempts to meet these needs including: a spin-on glass called HSQ (hydrogen silsesqui-oxane, HSiO.sub.1.5) and various carbon-based dielectric layers, such as parylene and amorphous fluorinated carbon. Other low-k films have been deposited by CVD using an organosilane precursor and oxygen to form a silicon-oxygen-carbon (Si--O--C) layer.

Brief Summary Text (5):
While the above types of dielectric films are useful for some applications, manufacturers are always seeking new and improved methods of depositing low-k materials for use as IMD and other types of dielectric layers. For example, in some applications, Si--O--C low-k films that have been deposited in accordance with the pre-deposition, deposition, post deposition, and curing processes described above are often subject to oxidizing environments in the course of subsequent processing. Such oxidizing processes include, but are not limited to, etching, photoresist strip and oxide capping processes. The low-k film is typically a silicon-oxy-carbon structure. In an oxidizing environment the low-k film can react with oxygen and hydrogen to form carbon dioxide (CO.sub.2) and water vapor (H.sub.2 O). The reaction removes carbon from the film leading to shrinkage and increase in k-value.

Detailed Description Text (29):
Certain embodiments of the present invention relate to deposition of a carbon-doped silicon oxide low K film using a thermal CVD process. Other embodiments of the present invention enhance the adhesion and stability of thin films including carbon-doped silicon oxide films deposited from an ozone/organosilane precursor gas according the method discovered by the present inventors. Embodiments of the invention can be practiced in a CVD deposition chamber such as the exemplary chamber described above. Embodiments of the present invention related to the deposition of a low k thermal CVD carbon-doped silicon oxide film are particularly useful for the deposition of premetal and intermetal dielectric layers (sometimes referred to as interlevel dielectric layers), especially those used for sub-0.2 micron applications.

Detailed Description Text (31):

The present inventors have found that the dielectric constant of carbon-doped silicon oxide film deposited in step 305 is directly related to the temperature of the substrate during deposition. In order to deposit a film having a dielectric constant that is sufficient for low k applications (e.g., a k less than or equal to 3.0), it is important that the deposition temperature be kept below 250.degree. C. Temperatures lower than 250.degree. C. are preferred in other embodiments.

Detailed Description Text (39):
In one embodiment, heater control subroutine maintains the chamber walls 15a at a temperature of approximately 60.degree. C. and lid assembly 15b at a temperature of approximately 25.degree. C. during deposition of a low-k material with an organosilane precursor. Operating the system in this manner inhibits thermal reaction of the precursor behind the blocker plate 42 and prevents choking of the flow of gas through the gas distribution manifold 11. Consequently, the deposition rate can be substantially increased compared to deposition performed with a single heat exchanger coupled to both lid assembly 15b and walls 15a. Heater control subroutine 87 can be configured to separately control heat exchangers H1 and H2.

Detailed Description Text (52):
Instead, the cure process can be performed in a conventional furnace with a relatively inert atmosphere, e.g., nitrogen, oxygen, or ammonia, or under vacuum conditions. In either case, the cure can be done in situ, i.e., without breaking vacuum, or ex situ, but ex situ processes are generally preferred since in situ processes require use of a relatively expensive deposition chamber and can significantly reduce throughput of the tool.

Detailed Description Text (54):
In a specific embodiment, a vacuum cure heats the substrate to a temperature of about 400.degree. C. for a period of about 10 minutes in a low pressure nitrogen environment. Such a process stabilizes the deposited film so that it resists moisture absorption in the future. The substrate may be transferred to another chamber, e.g. a different chamber in the same cluster tool as the deposition chamber, for curing without breaking vacuum. A specific embodiment of a conventional furnace cure also heats the substrate to a temperature of about 400.degree. C. for a period of about 30 minutes in a nitrogen atmosphere.

Detailed Description Text (63):
In other embodiments of the present invention, one or more dopants may optionally be included with the organosilane and ozone during deposition of the low-k layer for both PMD and IMD applications. For example phosphorous (P) may be added using, e.g., phosphine (PH.sub.3) during the deposition described above to getter alkali metals, e.g., sodium (Na), thereby reducing metal contamination of the deposited film. Boron may be added, e.g. using diborane (B.sub.2 H.sub.6). Boron tends to make the deposited film flow easily but also diffuses easily. Diffusion of Boron from the Si--O--C layer into an underlying silicon substrate might be useful for doping the silicon for making a device, such as a gate structure. Alternatively, both boron (B) and phosphorous may be added during deposition to produce a film that has a reduced viscosity and can be reflowed to achieve high aspect ratio gap-fill for

PMD applications.

Detailed Description Text (66):
In another version of this embodiment, the second step can be a PECVD process. For example, a Si--O--C type low-k film can be deposited by energizing a process gas mixture of an organosilane with nitrous oxide (N.sub.2 O) or O.sub.2 to form a deposition plasma. Suitable organosilanes include methylsilane, dimethylsilane (DMS), trimethylsilane (TMS), tetramethylsilane (T4MS) and phenylmethylsilane among others. The PECVD Si--O--C layer is under a compressive stress. The thermal deposited Si--O--C layer is under tensile stress. When the two layers are deposited on top of one another to form a combined film the compressive and tensile stresses tend to compensate for each other producing a low stress film. Such a low stress film would be resistant to cracking.

Detailed Description Text (68):
While the above described ozone/organosilane carbon-doped silicon oxide film is useful for a variety of applications, the present inventors have developed a number of pre-deposition and post-deposition steps that facilitate the integration of a low K ozone/organosilane carbon-doped silicon oxide film according to the present invention into established integrated circuit manufacturing processes. One example of such a multistep process is depicted in FIG. 10. As shown in FIG. 10, the process starts with a pre-deposition treatment 1000 to enhance the adhesion of the film to underlying aluminum. The pre-deposition treatment 1000 uses free atomic hydrogen to reduce an aluminum oxide that builds up on the aluminum. In a specific embodiment, free atomic hydrogen is dissociated from a hydrogen-containing gas in a remote source. In another specific embodiment, the remote source energizes the hydrogen containing gas with electromagnetic radiation. In a preferred embodiment the electromagnetic radiation is in the form of microwaves. Further details of predisposition step 1000 are described below in conjunction with FIGS. 11a and 11b.

Detailed Description Text (76):
As shown in FIG. 2, a remote source, fluidly coupled to the process chamber provides free atomic hydrogen for the pre-treatment. The remote source supplies energy that dissociates a hydrogen-containing gas such as ammonia (NH.sub.3) or molecular hydrogen (H.sub.2). Such a remote source can be a purely thermal source, in which hydrogen containing gas is dissociated by heating at a high temperature. More preferably, the remote source is a remote plasma source that dissociates hydrogen-containing gas in a plasma that is initiated and sustained with energy in the form of electromagnetic radiation. In this application, electromagnetic radiation is taken to mean any form of radiation resulting from oscillating electromagnetic fields. Such radiation includes but is not limited to all bands of the electromagnetic spectrum including long wave, radiofrequency, microwave, infrared, visible ultraviolet, x-ray and gamma ray. Still more preferably, the remote source dissociates hydrogen-containing gas with radiation having a frequency of between about 100 kilohertz (kHz) and 100 gigahertz (GHz). A strike gas such as argon (Ar) or nitrogen (N.sub.2) may optionally be supplied to the remote plasma source to facilitate striking the plasma.

Detailed Description Text (83):

After deposition, a silicon carbon or Si--O--C film is often quite porous. Consequently, the film tends to absorb moisture. The absorbed moisture generally degrades the properties of the film. In the case of a low-k film, moisture tends to increase the dielectric constant of the film and is detrimental to film adhesion. The porosity is normally reduced during the previously described thermal cure. However, if the cure is performed ex-situ, the film is exposed for a time to moisture from the ambient atmosphere (e.g., the clean room atmosphere). The film may also tend to shrink during subsequent polymerization and curing processes.

Detailed Description Text (84):
Additional modifications to the above described deposition process provide for a post deposition treatment to enhance adhesion of a low-k dielectric layer to a subsequently deposited layer and reduce shrinkage. The post-deposition treatment (step 1020 in FIG. 10) generally includes a densification step performed before removing the substrate from vacuum. The densification involves heating the substrate in a reducing ambient atmosphere to reduce shrinkage of the low-k dielectric layer. Suitable reducing environments include NH.sub.3 and H.sub.2. The densification can be performed in the same chamber as the deposition, or a different chamber. If done in a different chamber, however, the wafer is preferably transferred to that chamber under vacuum controlled conditions.

Detailed Description Text (86):
The densification described above is not normally employed in embodiments where the substrate is cured without breaking vacuum after depositing the low-k film. While the present inventors have found post deposition step 1020 to be particularly useful to stabilize low k ozone/organosilance carbon-doped silicon oxide films deposited according to the present invention and that are subsequently cured in an ex-situ process, step 1020 is a useful treatment for any film that is unstable in air. Such a densification is particularly useful for protecting low temperature deposited films that undergo an ex-situ cure. Such films include TMS-ozone films, spin on glass (SOG) and Black Diamond.TM.. In the case of Black Diamond.TM., the densification is performed in an oxygen (O.sub.2) ambient to remove hydrogen from the film.

Detailed Description Text (88):
Si--O--C low-k films that have been deposited in accordance with the pre-deposition, deposition, post deposition, and curing processes described above are often subject to oxidizing environments in the course of subsequent processing. Such oxidizing processes include, but are not limited to, etching, photoresist strip and oxide capping processes. The low-k film is typically a silicon-oxy-carbon structure. In an oxidizing environment the low-k film can react with oxygen and hydrogen to form carbon dioxide (CO.sub.2) and water vapor (H.sub.2 O). The reaction removes carbon from the film leading to shrinkage and increase in k-value.

Detailed Description Text (89):
The situation is illustrated in the Fourier transform infrared (FTIR) spectra depicted in FIGS. 13a-13d. FIG. 13a depicts a first FTIR spectra 1302 for an as-deposited Si--O--C low-k film. Note the presence of C--H and Si--C bonds in the spectra indicating the desired Si--O--C

structure. To simulate the effect of an oxidizing environment during processing, the as deposited film was subjected to an oxygen plasma for 3 minutes at 400.degree. C. The oxygen plasma produces active oxygen species that attack the film. A second FTIR spectra 1304 taken after oxygen plasma treatment shows little or no C--H and Si--C bonds indicating the removal of carbon from the film. The FTIR spectra in FIG. 13b. show that oxygen plasma also removes carbon from a post-cured Si--O--C film. Spectra 1306, for example, was taken on a post cured TMS-ozone deposited film. Spectra 1308 was taken on the same film after treatment in oxygen plasma for 3 minutes at 400.degree. C.

Detailed Description Text (92):
To overcome these problems, another embodiment of the method of the present invention includes a densification treatment after the film is cured. The densification process is an optional process that depends, to a certain extent, on the type of low-k film. For example, a densification step is not normally implemented for a barrier low-k (BLOK.TM.) film since this type of film has a silicon carbide (Si--C) structure that is not normally subject to oxidation. The plasma densification process is particularly useful for Si--O--C films deposited using an organosilane. Typically the densification plasma is an RF plasma containing helium (He), nitrogen (N.sub.2), or Argon (Ar). Alternatively an RF or remote microwave plasma containing NH.sub.3 and O.sub.2 may be used. Preferably, the plasma is formed from a gaseous mixture of He and N.sub.2. Ar plasma is not normally if sputtering would be a problem. However, Ar plasma may be used if, for example, sputtering is a desired effect.

Detailed Description Text (93):
In one embodiment, a substrate containing a TMS-ozone deposited low-k film is cured in-situ at approximately 400.degree. C. for between approximately 3 and 30 minutes, preferably about 10 minutes. The cured film is then subjected to N.sub.2 plasma for approximately two minutes while the substrate is heated to between approximately 350 and 450.degree. C., preferably about 400.degree. C. The chamber pressure is typically maintained at between about 1.2 and 5.0 torr, preferably about 1.5 torr. The plasma is sustained by radiofrequency (RF) energy delivered at a power of between 500 and 900 watts, preferably about 700 Watts and a frequency of between 100 KHz and 100 MHz, preferably about 450 KHz. One example of a suitable chamber for the densification process is a DxZ PECVD chamber manufactured by Applied Materials of Santa Clara, Calif. Such a chamber is described in U.S. Pat. No. 5,558,717.

Detailed Description Text (95):
As can be seen in FIG. 12e, the plasma densification process stabilizes the film and prevents removal of carbon in an oxidizing environment such as etch and photoresist strip. Table I demonstrates that the N.sub.2 treatment has a negligible effect on the refractive index (and therefore k-value) of the film. Table I further demonstrates that the N.sub.2 densification process produces relatively little shrinkage of the post cured film.

Detailed Description Text (96):
Furthermore, the present inventors have discovered that if an overlying cap layer is deposited over an ozone/organosilane film according to the present invention, densification treatment 1040 prevents delamination

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DATE: Sunday, December 12, 2004

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☐	L13	L12 and uv	1
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☐	L5	L1 and ((drying or remov$) same (uv or ultraviolet) same temperature same vacuum)	0
☐	L4	L3 and temperature and vacuum	65
☐	L3	L1 and ((drying or remov$) same (uv or ultraviolet))	117
☐	L2	L1 and drying	156
☐	L1	low k dielectric	1685

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L8: Entry 8 of 9 File: USPT May 7, 2002

DOCUMENT-IDENTIFIER: US 6383913 B1
TITLE: Method for improving surface wettability of low k material

Detailed Description Text (6):
Then, in one embodiment, the characteristic of the low-k barrier layer 16 is modified from hydrophobic to less hydrophobic or said more hydrophilic by UV treatment. UV treatment can improve the surface adhesion of inorganic dielectric material as a low-k barrier layer compatible with organic polymer. In another embodiment, an adhesion promoter also can be coated on the low-k barrier layer 16 by spin-on method with thickness less than 200 angstroms. Then, the adhesion promoter is baked at temperature between about 100 to 200.degree. C. To remove the remained solvents on the adhesion promoter, then, a second low-k dielectric layer 18 is formed the first low-k barrier layer 16. Later, a first photoresist layer is deposited, exposed, and developed by the use of known techniques to form an opening 24 (shown in FIG. 2) to define a subsequent via opening.

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of an overlying cap layer due to bubble formation. Bubbles may form with an undensified Si--O--C layer due to outgassing from the Si--O--C layer during high temperature processes such as annealing. In an experiment, a low-k film was deposited on a substrate using TMS-ozone as described above. After deposition, the substrate was cured for 5 minutes at 400.degree. C. After curing, the substrate was subject to N.sub.2 plasma for 2 minutes and then capped with PE TEOS. The substrate exhibited no bubbling of the cap layer even after annealing at 450.degree. C.

Detailed Description Text (99):
To overcome this, another embodiment of the present invention includes capping the TMS-ozone deposited low-k film with a layer of oxide or nitride. It is believed that the if the cap layer is harder than TMS-ozone low-k layer the cap layer physically holds the low-k film together. The cap layer provides a barrier against moisture penetration of the low-k film. The cap layer, typically a silicon oxide or silicon nitride, may be deposited by any conventional means. Preferably the cap layer is a silicon oxide deposited to a thickness of between 1000 .ANG. and 3000 .ANG. by plasma enhanced chemical vapor deposition (PECVD) using a precursor such as TEOS. Such a cap layer is referred to herein as a PE TEOS layer. The inventors have found that a TMS-ozone film that has been plasma densified and capped with a 1000 .ANG. PE TEOS film is stable up to a thickness of 1.6 microns. At about 2 microns thick, a densified and cupped film cracks after 3-4 days. Silicon nitride generally provides a stronger cap layer and a better moisture barrier. Consequently, silicon nitride cap layers can be thinner, perhaps for example, or the order of a few hundred angstroms.

Detailed Description Text (107):
The flow diagram of FIG. 14d shows the details of an exemplary furnace cure, shown in FIG. 10 as step 1030. In the exemplary embodiment, the substrate is removed from a vacuum environment and placed in a furnace in step 1431. Of course, multiple wafers may be placed in the furnace for simultaneous curing. Substrate process throughput is generally optimized when as many substrates as possible are furnace cured at the same time. An ambient atmosphere of nitrogen (N.sub.2) is provided to the furnace at step 1432. The furnace then heats the substrate to a temperature of about 400.degree. C. for a period of about 30 minutes in step 1433.

Detailed Description Text (110):
The flow diagram of FIG. 14g shows the details of an exemplary capping step, shown in FIG. 10 as step 1050. In the exemplary embodiment, the cap layer is deposited on the plasma densified Si--O--C layer in the same chamber as that used in the plasma densification step. Alternatively, the substrate containing the Si--O--C film may be transferred to a different chamber for capping. In step 1451, process gas flows and other process conditions are established. Helium is provided at about 1000 sccm. TEOS is provided at about 1050 milligrams/minute (mgm). Oxygen (O.sub.2) is provided at about 1000 sccm. The chamber pressure is generally about 8.2 torr and the pedestal temperature about 400.degree. C. In step 1452 the process gases are energized to form a plasma. 1000 Watts of RF power are supplied at a frequency of about 13.56 MHz. In step 1453 a silicon oxide cap layer is deposited using the plasma. Deposition proceeds until the cap layer has a thickness of about 2000 .ANG.. In step 1454, RF power is turned off

and the flow of process gases is stopped. The substrate may then be removed from the chamber for further processing, such as photoresist deposition, metal deposition, etc.

Detailed Description Text (111):
The methods described above can be readily incorporated into existing process recipes. For example, FIGS. 15a-15h depict one example of an IMD gap fill process incorporating the above method. In FIG. 15a a first metal layer 1502 of Al is deposited on an Si substrate 1500. An anti-reflective coating of TiN 1504 is deposited on Al layer 1502. In FIG. 15b a first photoresist layer 1506 is deposited on the TiN 1504. The walls of gaps 1508 are treated with free atomic hydrogen as described above to reduce aluminum oxide. In FIG. 15c TiN and Al layers are etched to form gaps 1508 using the patterned photoresist 1506. In FIG. 15d A low-k TMS layer 1510 is deposited, cured and densified as described above to fill gaps 1508. TMS layer 1510 is capped with PE TEOS 1512. PE TEOS layer 1512 is planarized (e.g., using CMP) and covered with a second patterned photoresist 1514 in FIG. 15e. PE TEOS and TMS layers are then etched through second patterned photoresist layer 1514 down to TiN layer 1504 to form vias 1516 as shown in FIG. 15f. After etching, photoresist 1514 is stripped, e.g., by ashing in an oxidizing environment. Densification treatment 1040 protects PE TEOS and TMS layers during etch and photoresist strip. Vias 1516 are filled with a metal such as tungsten to form interconnects 1518 as shown in FIG. 15g. After planarization, a second metal layer 1520 and barrier layer 1522 can be deposited over interconnects 1518 as shown in FIG. 15h. The process of FIGS. 15b-15h can then be repeated multiple times until the desired integrated circuit structure is complete. Such a process integration scheme is simple and involves relatively little complexity with CMP, etch, and photoresist strip. Such a process does produce relatively high k values between the metal layers due to PE TEOS layer 1512. Lower k values between the lines can be achieved, for example by eliminating the deposition of PE TEOS cap layer 1512.

Detailed Description Text (112):
A dual-damascene process integration scheme that utilizes the low-k TMS-ozone deposition method described herein is depicted in FIGS. 16a-16h. The dual damascene process begins with the deposition of an oxide layer 1602 over a silicon substrate 1600 as shown in FIG. 16a. A hardmask layer 1604, e.g., silicon nitride (Si.sub.3 N.sub.4), is deposited over oxide layer 1602. A first low-k TMS layer 1606 is deposited, cured and densified as described above. First TMS layer 1606 is covered with a patterned photoresist layer 1608 during a first photolithography as shown in FIG. 16b. In FIG. 16c, a first etch forms a first set of gaps 1610 in first TMS layer 1606 down to hardmask layer 1604. After the first etch, photoresist 1608 is stripped, e.g., by ashing in an oxidizing environment. Densification treatment 1040 protects TMS layer 1606 during etch and photoresist strip. Gaps 1610 and first TMS layer 1606 are then covered with a layer of metal, such as aluminum or copper. In the case of copper, a seed layer 1612 (FIG. 16c) is deposited over gaps 1610 and first TMS layer 1606. A first bulk copper layer 1614 is deposited to fill the gaps 1610 as shown in FIG. 16d. Copper layer 1614 is planarized, e.g., by CMP. Copper layer 1614 forms, e.g., a first set of metal lines in an interconnect structure.

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L20: Entry 21 of 39 File: USPT May 6, 2003

DOCUMENT-IDENTIFIER: US 6559045 B2
TITLE: Fabrication of integrated circuits with borderless vias

Brief Summary Text (5):
As feature sizes in the production of integrated circuits approach 0.25 .mu.m and below, problems of packing density become increasingly difficult to overcome. The formation of borderless vias is one method to reduce metal pitch in and packing density of integrated circuits. However, it is exceedingly difficult to form borderless vias in conventional subtractive interconnect patterning. The major problem is that deep and narrow trenches are produced at the side of metal lines in via etching whenever vias are misaligned to the underlying metal lines. The trench depth is extremely difficult to control since it is common practice to excess plasma etch in via etch to ensure that via holes are completely open. Organic byproducts are produced in dielectric plasma etching when opening via holes. Those byproducts accumulated at the bottom of trenches cannot be effectively removed by oxygen-based plasma or ashing which are commonly used techniques to strip photoresist used in integrated circuit fabrication. Liquid organic chemicals, which are also commonly used to remove organic byproducts, often cause corrosion of metals from which interconnects are made. As a result, via resistance can be very high and, thus, the performance and reliability of integrated circuits degrade. In extreme cases, integrated circuits fail to function when via holes are totally blocked and vias become electrically open.

Brief Summary Text (6):
The cause of the above mentioned issues of conventional architectures is the lack of a etchstop or plasma etch selectivity when opening vias. These occur in two different ways. First, the same kind of inorganic dielectric is typically used for the via-level and metal-level inter-level dielectrics (IMD.quadrature.). Even when two different kinds of inorganic dielectrics are used, as far as plasma etching for via holes is concerned, the difference between these two kinds of inorganic dielectrics is insignificant. As a result, via etch continues even when via holes are already fully opened as long as there is misalignment between via and the underlying interconnects or metal lines. The use of two different kinds of dielectrics, one inorganic and the other organic, have been used for the metal-level and the via-level IMD.quadrature., respectively, in some prior architectures. This architecture does not have the aforesaid disadvantage architectures since there is very high plasma etch selectivity between inorganic and organic dielectrics. However, its weakness is associated with the photoresist, which is commonly used for patterning, a key technique in integrated circuit fabrication. In conventional integration methods, both the photoresist and the organic IMD.quadrature. are exposed at the

completion of via etch. The organic via-level dielectric is attacked, resulting in deep trenches along the side of metal lines when removing the photoresist which is also organic.

Brief Summary Text (7):
According to the invention one ensures that the part of the via-level IMD, which is exposed to via etch plasma due to misalignment between via and metal lines, does not etch or only insignificantly etches in via openings and during resist removal following via etch. The invention provides borderless vias in integrated circuits. Two key elements are the use of dielectrics of significantly dissimilar plasma etch characteristics and that the dielectric immediately over metal lines is different from the dielectric at the sidewall of the metal lines. These objectives are achieved by dividing the metal-level IMD into two parts. One dielectric on the sidewall of the metal lines and the rest of the metal-level IMD between the dielectric on the side walls. The two dielectrics are significantly different from each other in their plasma etch characteristics. Another embodiment adds a hardmask layer between a photoresist layer and the organic dielectric for the via-level IMD so that either resist or the organic dielectric can be selectively removed. A hardmask is also necessary when the via-level IMD is inorganic and the etchstop, at the sidewall of metal lines, in via etch is organic. The hardmask can be either permanent or sacrificial. Performance enhancement of integrated circuits is achieved with the implementation of new architectures according to this invention in conjunction with the use of dielectrics of low dielectric constant.

Brief Summary Text (11):
The invention further provides a process for producing an integrated circuit structure which comprises (a) providing a substrate; (b) depositing a layer of a second dielectric material on the substrate; (c) forming a pattern of metal contacts on the layer of the second dielectric material; (d) conformally depositing a lining of a first dielectric material on side walls of the metal contacts, on a top surface of the metal contacts, and on a floor of a space between the metal contacts on the layer of the second dielectric material; (e) removing the first dielectric material from the top surface of the metal contacts while retaining the first dielectric material lining on the side walls of the metal contacts; (f) depositing an additional layer of the second dielectric material on the top surface of the metal contacts and in the space between adjacent linings of the metal contacts; (g) depositing a layer of a sacrificial metal on the additional layer of the second dielectric material; (h) depositing a layer of a photoresist on the layer of the sacrificial metal layer; (i) imagewise removing a portion of the photoresist over at least one metal contact and optionally over at least a portion of the lining of first dielectric material on a side wall of a metal contact; (j) removing the portion of the layer of the sacrificial metal under the removed portion of the photoresist; (k) removing the balance of the photoresist layer, and removing the portion of the additional layer of the second dielectric material under the removed portion of the sacrificial metal layer until at least one metal contact and optionally a lining on a side wall of a metal contact is reached thus forming at least one via through the second dielectric material extending to at least one metal contact and optionally a lining of a side wall of a metal contact.

Brief Summary Text (13):
The invention still further provides a process for producing an integrated circuit structure which comprises (a) providing a substrate; (b) depositing a layer of a third dielectric material on the substrate; (c) forming a pattern of metal contacts on the layer of the third dielectric material; (d) conformally depositing a lining of a first dielectric material on side walls of the metal contacts, on a top surface of the metal contacts, and on a floor of a space between the metal contacts on the layer of the third dielectric material; (e) removing the first dielectric material from the top surface of the metal contacts while retaining the first dielectric material lining on the side walls of the metal contacts; (f) depositing a layer of a second dielectric material on the top surface of the metal contacts and in the space between adjacent linings of the metal contacts; (g) depositing an additional layer of the third dielectric material on the layer of the second dielectric material; (h) depositing a layer of a photoresist on the additional layer of the third dielectric material; (i) imagewise removing a portion of the photoresist over at least one metal contact and optionally over at least a portion of the lining of first dielectric material on a side wall of a metal contact; (j) removing the portion of the additional layer of the third dielectric material under the removed portion of the photoresist, (k) removing the balance of the photoresist layer, and removing the portion of the second dielectric material under the removed portion of the additional layer of the third dielectric material until at least one metal contact and optionally a lining on a side wall of a metal contact is reached thus forming at least one via through the second dielectric material extending to at least one metal contact and optionally a lining of a side wall of a metal contact.

Detailed Description Text (4):
This structure uses two different kinds of low-k dielectric thin films for the IMD. One of Dielectric I and Dielectric II is organic and the other is inorganic. That is, if Dielectric I is organic then Dielectric II is inorganic and if Dielectric I is inorganic then Dielectric I is organic. The process steps used for the fabrication of the via and metal levels can be repeated again for the upper levels of vias and metals. The advantage of the invention is a significant difference in plasma etch rate between organic and inorganic dielectrics. This is not possible when the same dielectric is employed for both via-level and metal-level IMD.quadrature.. In oxygen-based plasmas, organic dielectrics etch tremendously faster than inorganic dielectrics. Inversely, in carbon fluoride based plasmas, inorganic dielectrics etch much faster than organic dielectrics.

Detailed Description Text (5):
A first process embodiment of the invention for producing the architecture of FIG. 2A is exemplified by FIGS. 3A through 3I. These figures show the process flow after the formation of the one interconnect level, however, the same processing steps can be repeated again for upper levels of vias and interconnects. FIG. 3A shows the interim structure at a beginning step which is a deposition of an organic low-k dielectric (Dielectric II) onto a substrate and forming a pattern of metal contacts on the layer of the second dielectric material. Typical substrates include those suitable to be processed into an integrated circuit or other microelectronic device. Suitable substrates for the present invention non-exclusively include

semiconductor materials such as gallium arsenide (GaAs), germanium, silicon, silicon germanium, lithium niobate and compositions containing silicon such as crystalline silicon, polysilicon, amorphous silicon, epitaxial silicon, and silicon dioxide (SiO.sub.2) and mixtures thereof. The metal contact lines are typically formed by well known lithographic techniques. Suitable materials for the lines include aluminum, aluminum alloys, copper, copper alloys, titanium, tantalum, and tungsten. These lines form the conductors of an integrated circuit. Such are typically closely separated from one another at distances preferably of from about 20 micrometers or less, more preferably from about 1 micrometer or less, and most preferably of from about 0.05 to about 1 micrometer.

Detailed Description Text (16):
The dielectrics may optionally be heated to expel residual solvent or to increase its molecular weight. The heating may be conducted by conventional means such as heating on a hot plate in air or in an inert atmosphere, or it may occur in a furnace or oven in air, or in an inert atmosphere, or it may occur in a vacuum furnace or vacuum oven. Heating is preferably conducted at a temperature of from about 80.degree. C. to about 500.degree. C., and more preferably from about 150.degree. C. to about 425.degree. C. This heating is preferably performed from about 1 minute to about 360 minutes, and more preferably from about 2 to about 60 minutes. The dielectric layer may also optionally be exposed to actinic light, such as UV light, to increase its molecular weight. The amount of exposure may range from about 100 mJ/cm.sup.2 to about 300 mJ/cm.sup.2. The dielectric layers may optionally be cured by overall exposed to electron beam radiation. Electron beam exposure may be controlled by setting the beam acceleration. Electron beam radiation may take place in any chamber having a means for providing electron beam radiation to substrates placed therein. It is preferred that the electron beam exposing step is conducted with a wide, large beam of electron radiation from a large-area electron beam source. Preferably, an electron beam chamber is used which provides a large area electron source. Suitable electron beam chambers are commercially available from Electron Vision, a unit of AlliedSignal Inc., under the trade name .quadrature.lectronCure.TM.". The principles of operation and performance characteristics of such device are described in U.S. Pat. No. 5,003,178, the disclosure of which is incorporated herein by reference. The temperature of the electron beam exposure preferably ranges from about 20.degree. C. to about 450.degree. C., more preferably from about 50.degree. C. to about 400.degree. C. and most preferably from about 200.degree. C. to about 400.degree. C. The electron beam energy is preferably from about 0.5 KeV to about 30 KeV, and more preferably from about 3 to about 10 KeV. The dose of electrons is preferably from about 1 to about 50,000 .mu.C/cm.sup.2 and more preferably from about 50 to about 20,000 .mu.C/cm.sup.2. The gas ambient in the electron beam tool can be any of the following gases: nitrogen, oxygen, hydrogen, argon, a blend of hydrogen and nitrogen, ammonia, xenon or any combination of these gases. The electron beam current is preferably from about 1 to about 40 mA, and more preferably from about 5 to about 20 mA. Preferably, the electron beam exposing step is conducted with a wide, large beam of electron beam radiation from a uniform large-are electron beam source which covers an area of from about 4 inches to about 256 square inches.

Detailed Description Text (19):

After imagewise removing a portion of the photoresist over at least one metal contact and optionally over at least a portion of the lining of first dielectric material on a side wall of a metal contact, the structure of FIG. 3E is obtained. This figure shows the structure after imagewise patterning and removal of portions of the resist in step 6. Such is formed in a manner well known in the art such as by imagewise exposing the photoresist to actinic radiation such as through a suitable mask and developing the photoresist. The photoresist may be imagewise exposed to actinic radiation such as light in the visible, ultraviolet or infrared regions of the spectrum through a mask, or scanned by an electron beam, ion or neutron beam or X-ray radiation. Actinic radiation may be in the form of incoherent light or coherent light, for example, light from a laser. The photoresist is then imagewise developed using a suitable solvent, such as an aqueous alkaline solution. Optionally the photoresist is heated to cure the image portions thereof and thereafter developed to remove the nonimage portions and define a via mask.

Detailed Description Text (20):
In step 7, after removing the portion of the layer of the sacrificial metal under the removed portion of the photoresist, the structure of FIG. 3F is attained. This is done by anisotropic sacrificial metal etch. The etch, preferably done in chlorine-based plasma chemistry, and stops by itself on reaching the underlying organic dielectric due to a significantly high etch selectivity between metal and the organic dielectric.

Detailed Description Text (25):
A process sequence for the production of the structure of FIG. 2C is shown via FIGS. 5A through 5G. These figures show the process flow after the formation of the one interconnect level, however, the same processing steps can be repeated again for upper levels of vias and interconnects. FIG. 5A shows the interim structure at a beginning step which is a deposition of an inorganic low-k third dielectric (Dielectric III) onto a substrate and forming a pattern of metal contacts on the layer of the second dielectric material. Typical materials for the substrates and metal contact lines have been described above. Deposition of the third dielectric onto the substrate may be conducted via conventional spin-coating, dip coating, roller coating, spraying, chemical vapor deposition methods, or meniscus coating methods which are well-known in the art. Spin coating is most preferred. The thickness of the dielectric layers may vary depending on the deposition procedure and parameter setup, but typically the thickness may range from about 500 .ANG. to about 50,000 .ANG., and preferably from about 2000 .ANG. to about 12000 .ANG.. In the preferred embodiment, a liquid dielectric composition is spun onto the appropriate surface according to known spin techniques such as by applying a liquid dielectric composition to the surface and then spinning on a rotating wheel at speeds ranging from about 500 to about 6000 rpm for about 5 to about 60 seconds. The layer preferably has a density of from about 1 g/cm.sup.3 to about 3 g/cm.sup.3.

Detailed Description Text (28):
The dielectrics may optionally be heated to expel residual solvent or to increase its molecular weight as described above. The dielectric layer may also optionally be exposed to actinic light, such as UV light, to increase its molecular weight or cured by overall exposed to

electron beam radiation as described above.

Detailed Description Text (32):
After imagewise removing a portion of the photoresist over at least one metal contact and optionally over at least a portion of the lining of first dielectric material on a side wall of a metal contact, the structure of FIG. 5E is obtained. This figure shows the structure after imagewise patterning and removal of portions of the resist in step 6. Such is formed in a manner well known in the art such as by imagewise exposing and developing the photoresist as described above.

Detailed Description Text (33):
In step 7, after removing the portion of the additional layer of Dielectric III under the removed portion of the photoresist, the structure of FIG. 5F is attained. This is done by anisotropic etch of Dielectric III. The etch stops on reaching the underlying organic dielectric due to a significantly high etch selectivity between Dielectric III and Dielectric II.

Detailed Description Text (37):
This structure again uses two different kinds of low-k dielectric thin films for the IMD. One of Dielectric I and Dielectric II is organic and the other is inorganic. That is, if Dielectric I is organic then Dielectric II is inorganic and if Dielectric I is inorganic then Dielectric I is organic. The process steps used for the fabrication of the via and metal levels can be repeated again for the upper levels of vias and metals. The advantage of the invention is a significant difference in plasma etch rate between organic and inorganic dielectrics.

Detailed Description Text (38):
A first process embodiment of the invention for producing the architecture of FIG. 2E is exemplified by FIGS. 7A through 7J. These figures show the process flow after the formation of the one interconnect level, however, the same processing steps can be repeated again for upper levels of vias and interconnects. FIG. 7A shows the interim structure at a beginning step which is a deposition of an inorganic low-k dielectric (Dielectric II) onto a substrate and forming a pattern of metal contacts on the layer of the second dielectric material. Typical substrates are those mentioned above.

Detailed Description Text (43):
After imagewise removing a portion of the photoresist over at least one metal contact and optionally over at least a portion of the lining of first dielectric material on a side wall of a metal contact, the structure of FIG. 7E is obtained. This figure shows the structure after imagewise patterning and removal of portions of the resist in step 6. Such is formed in a manner described above. Resist removal is done before the organic dielectric at the bottom of the vias are exposed by via etching. Embodiment I and Embodiment II, having an organic IMD and an inorganic etchstop at via etch, do not have this step. The difference arises from the fact that Embodiment V uses an organic etchstop, which can be exposed only after the resist has been removed first. In step 7, after removing the portion of the layer of the sacrificial metal under the removed portion of the photoresist, the structure of FIG. 7F is attained. This is done by anisotropic sacrificial metal etch as described. In step 8 the balance of the

resist is then stripped away to produce the structure of FIG. 7G.

CLAIMS:

1. A process for producing an integrated circuit structure which comprises (a) providing a substrate; (b) depositing a layer of a second dielectric material on the substrate; (c) forming a pattern of metal contacts on the layer of the second dielectric material; (d) conformally depositing a lining of a first dielectric material on side walls of the metal contacts, on a top surface of the metal contacts, and on a floor of a space between the metal contacts on the layer of the second dielectric material; (e) removing the first dielectric material from the top surface of the metal contacts while retaining the first dielectric material lining on the side walls of the metal contacts; (f) depositing an additional layer of the second dielectric material on the top surface of the metal contacts and in the space between adjacent linings of the metal contacts; (g) depositing a layer of a sacrificial metal on the additional layer of the second dielectric material; (h) depositing a layer of a photoresist on the layer of the sacrificial metal layer; (i) imagewise removing a portion of the photoresist over at least one metal contact and optionally over at least a portion of the lining of first dielectric material on a side wall of a metal contact; (j) removing the portion of the layer of the sacrificial metal under the removed portion of the photoresist; (k) removing the balance of the photoresist layer, and removing the portion of the additional layer of the second dielectric material under the removed portion of the sacrificial metal layer until at least one metal contact and optionally a lining on a side wall of a metal contact is reached thus forming at least one via through the second dielectric material extending to at least one metal contact and optionally a lining of a side wall of a metal contact.

13. A process for producing an integrated circuit structure which comprises (a) providing a substrate; (b) depositing a layer of a third dielectric material on the substrate; (c) forming a pattern of metal contacts on the layer of the third dielectric material; (d) conformally depositing a lining of a first dielectric material on side walls of the metal contacts, on a top surface of the metal contacts, and on a floor of a space between the metal contacts on the layer of the third dielectric material; (e) removing the first dielectric material from the top surface of the metal contacts while retaining the first dielectric material lining on the side walls of the metal contacts; (f) depositing a layer of a second dielectric material on the top surface of the metal contacts and in the space between adjacent linings of the metal contacts; (g) depositing an additional layer of the third dielectric material on the layer of the second dielectric material; (h) depositing a layer of a photoresist on the additional layer of the third dielectric material; (i) imagewise removing a portion of the photoresist over at least one metal contact and optionally over at least a portion of the lining of first dielectric material on a side wall of a metal contact; (j) removing the portion of the additional layer of the third dielectric material under the removed portion of the photoresist; (k) removing the balance of the photoresist layer, and removing the portion of the second dielectric material under the removed portion of the additional layer of the third dielectric material until at least one metal contact and optionally a lining on a side wall of a metal contact is reached thus forming at least one via

through the second dielectric material extending to at least one metal contact and optionally a lining of a side wall of a metal contact.

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